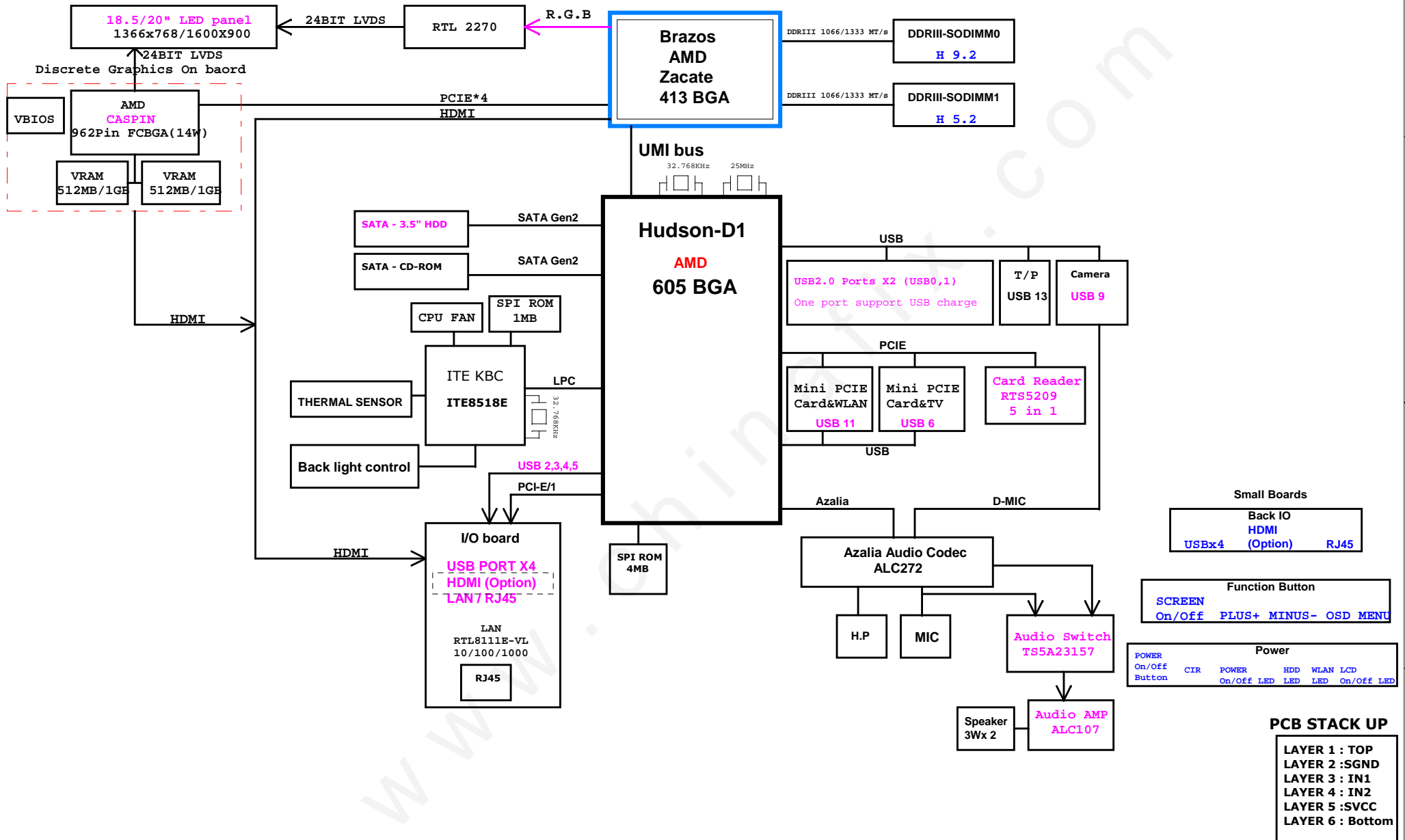
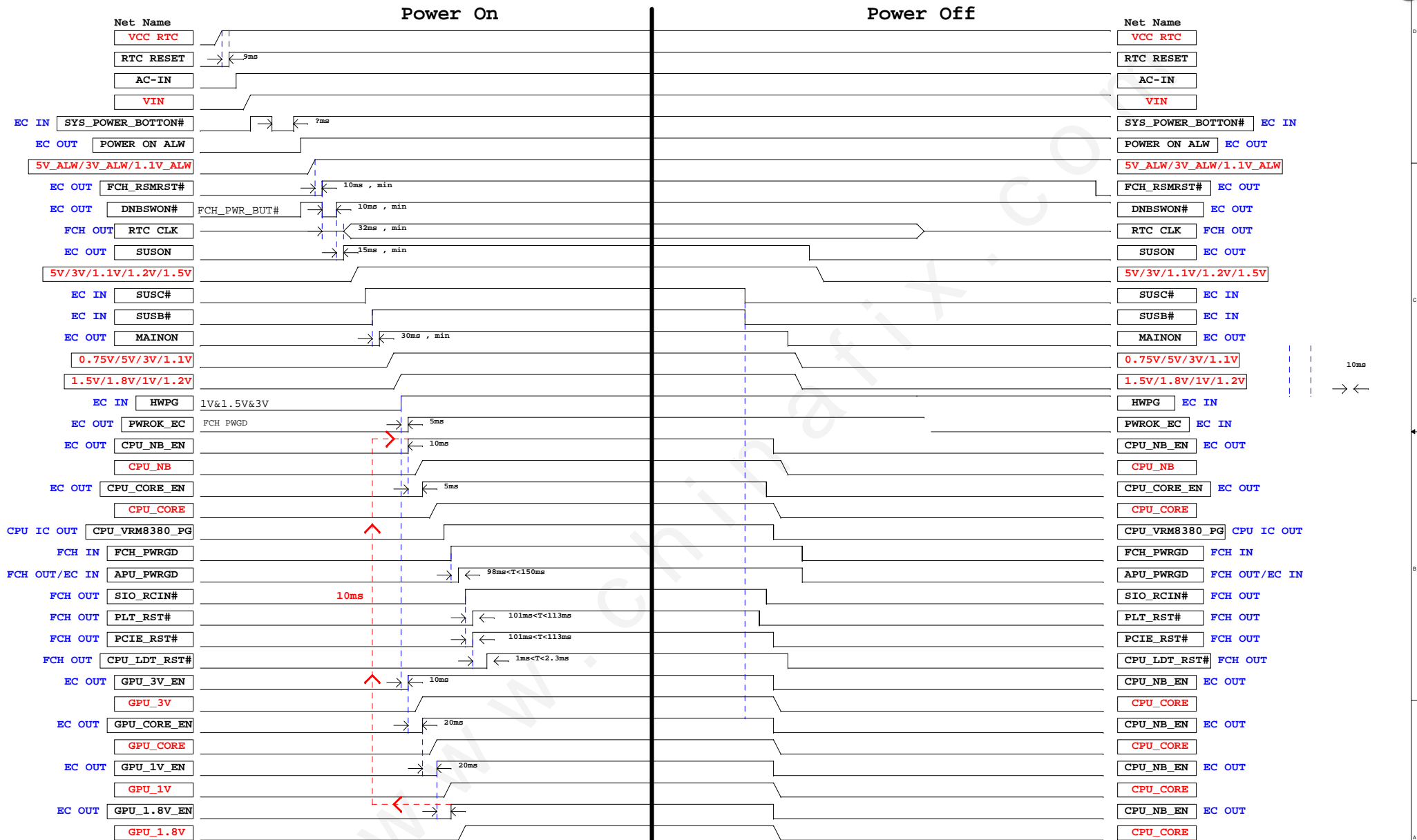


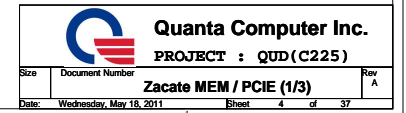
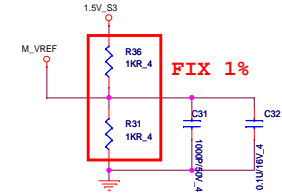
C325/C225 Brazos BLOCK DIAGRAM

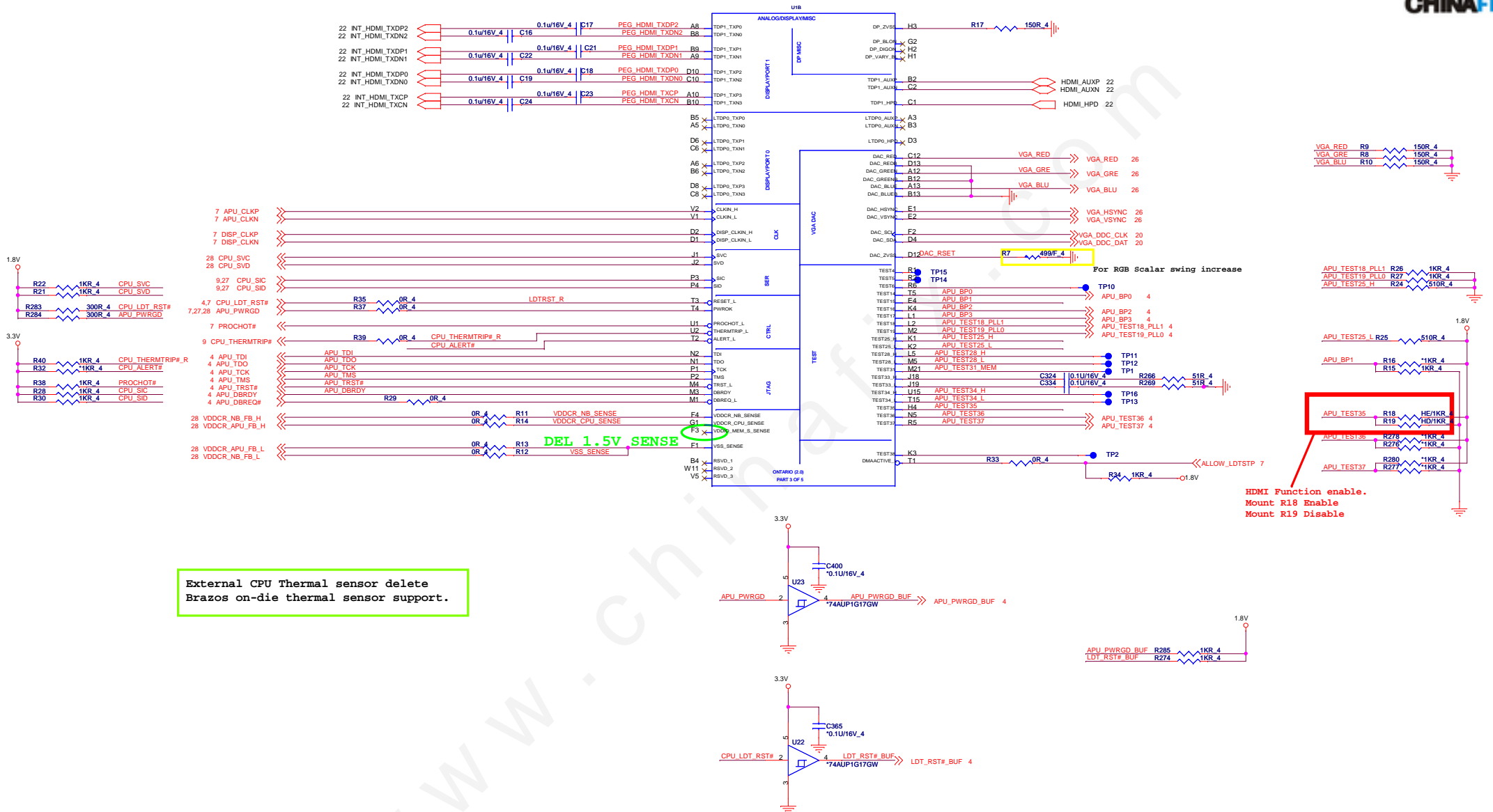


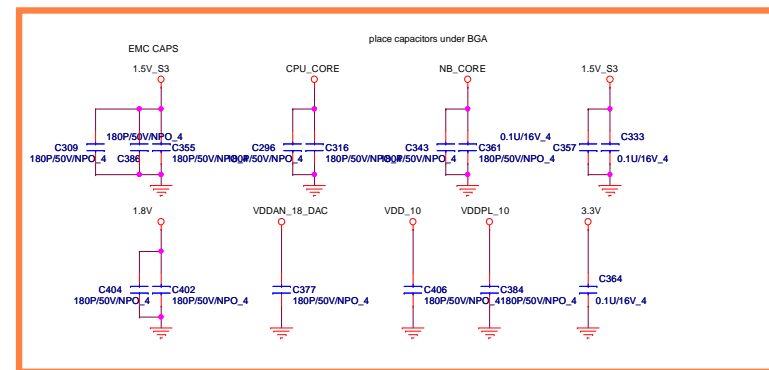
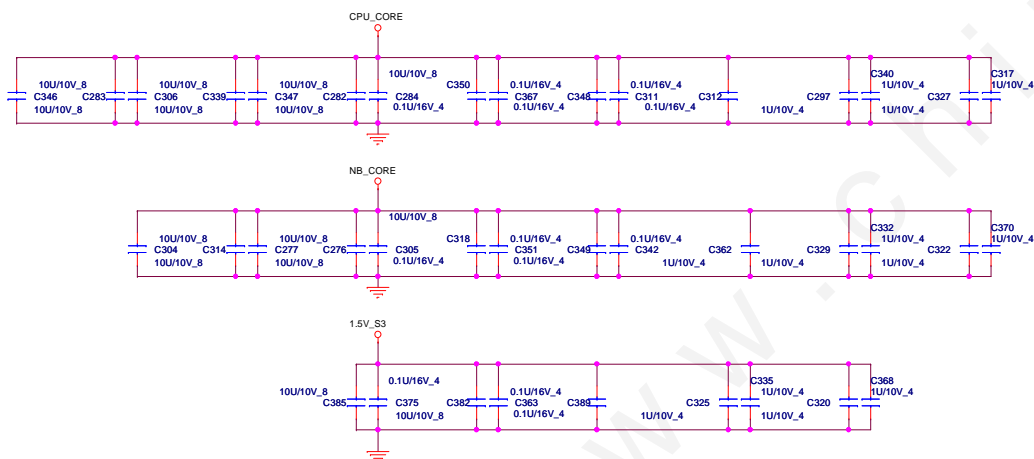
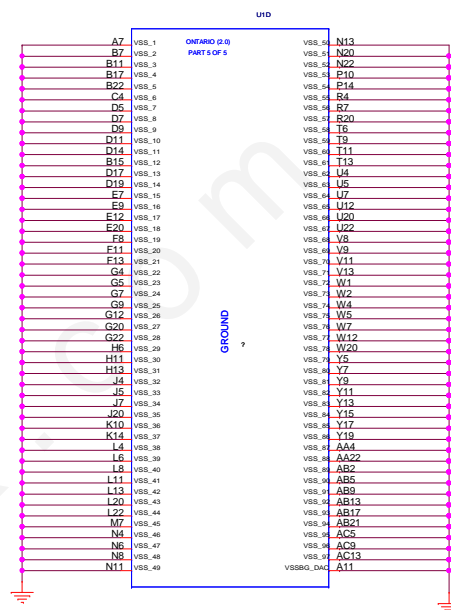
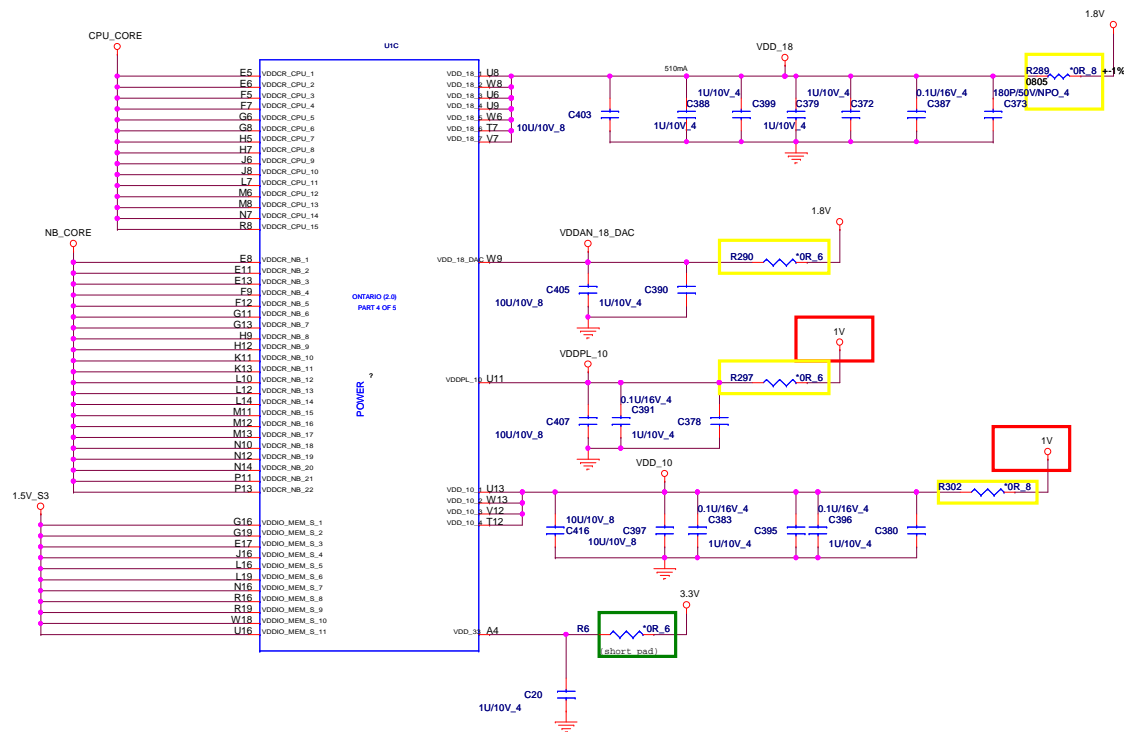
Power	Voltage	S9	S3	S4	S5	CS Signal
VCCDET	3V	ON	ON	ON	ON	ON
VIN	20V	ON	ON	ON	ON	OFF
5V_AUX	5V	ON	ON	ON	ON	ON
5V_AUX	5V	ON	ON	ON	ON	OFF
2V_S5	3.3V	ON	ON	OFF	OFF	OFF
1.5V_S5	1.1V	ON	ON	OFF	OFF	OFF
5V_S3	5V	ON	ON	OFF	OFF	ON
5V_S3	3.3V	ON	ON	OFF	OFF	ON
1.5V_S3	1.1V	ON	ON	OFF	OFF	ON
1.5V_S3	1.1V	ON	ON	OFF	OFF	ON
5V	5V	ON	OFF	OFF	OFF	ON
2V	3.3V	ON	OFF	OFF	OFF	ON
1.8V	1.8V	ON	OFF	OFF	OFF	ON
1.5V	1.5V	ON	OFF	OFF	OFF	ON
1.2V	1.2V	ON	OFF	OFF	OFF	ON
1.1V	1.1V	ON	OFF	OFF	OFF	ON
1V	1.05V	ON	OFF	OFF	OFF	ON
BRD_VTERR	0.72V	ON	OFF	OFF	OFF	ON
CMC_CORE	ON	ON	OFF	OFF	OFF	ON
MB_CORE	ON	ON	OFF	OFF	OFF	ON
VISA_CORE	1.05V	ON	OFF	OFF	OFF	ON
1.5VGA	1.8V	ON	OFF	OFF	OFF	ON
1.5VGA	1.5V	ON	OFF	OFF	OFF	ON
1.5VGA	1V	ON	OFF	OFF	OFF	ON

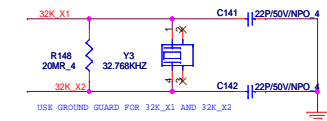
QUC Power On/Off Sequencing Timing Diagram



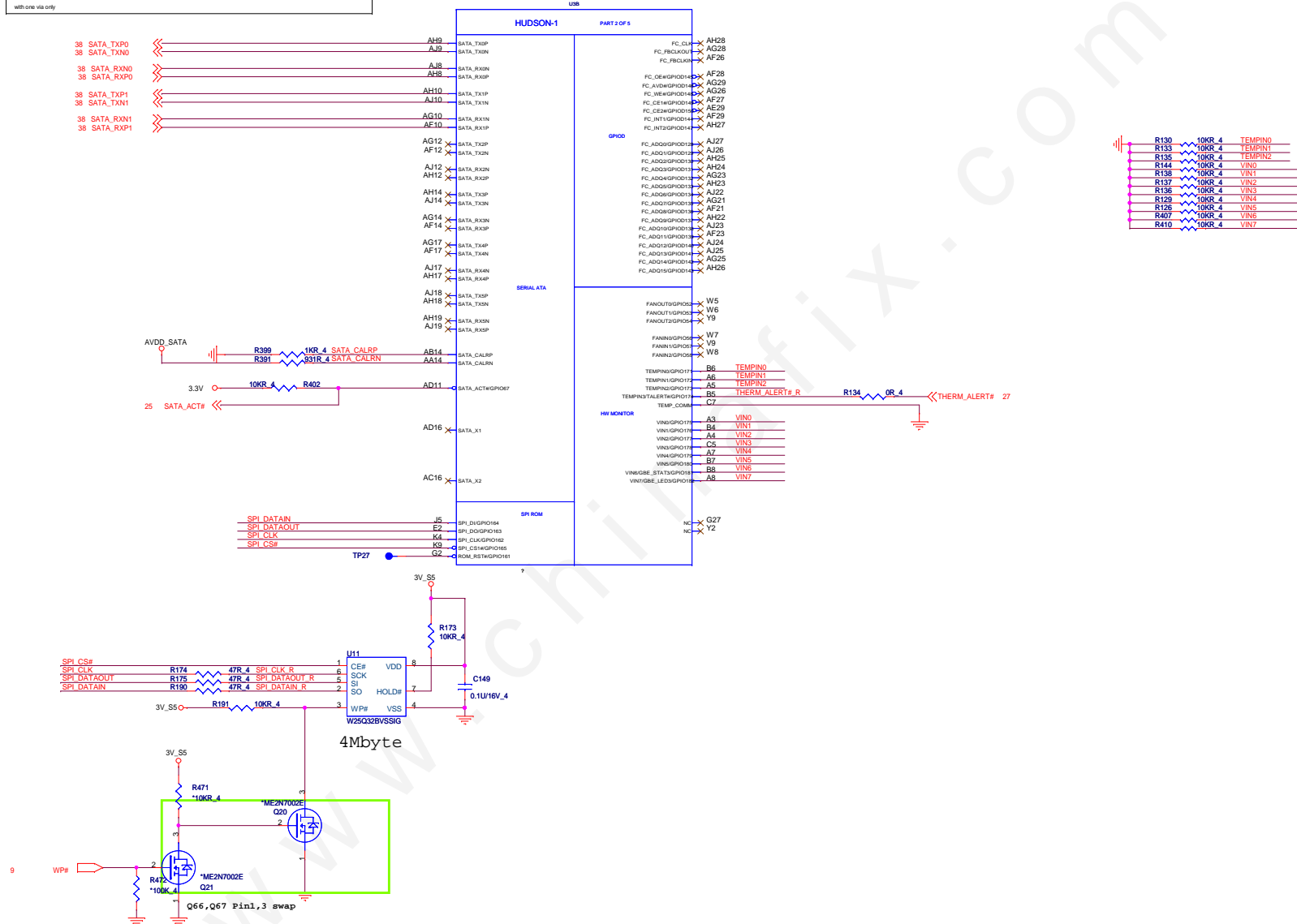




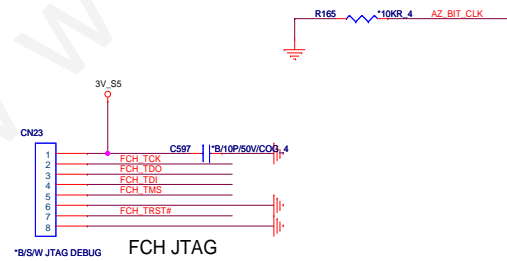
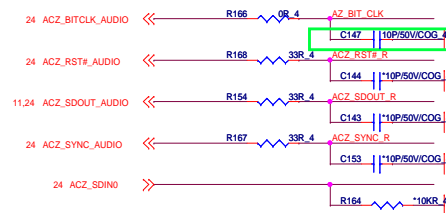
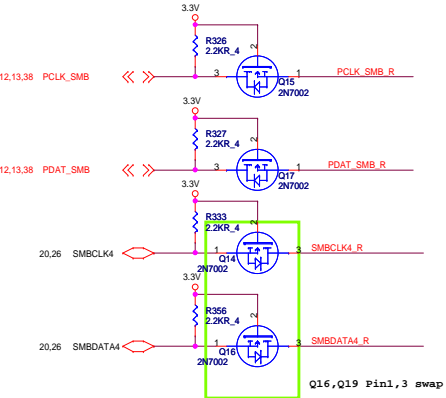
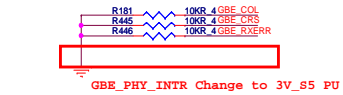
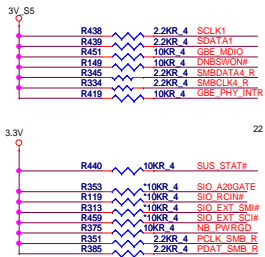




HDD

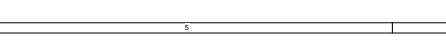
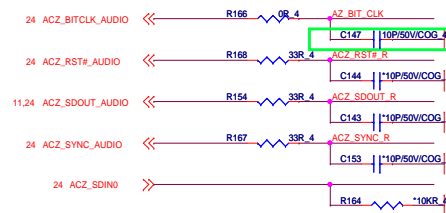


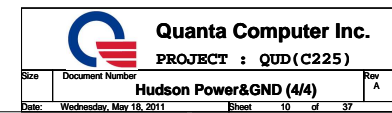
3V_S5 NC only ,Can't be install



FCH JTAG

Reserve

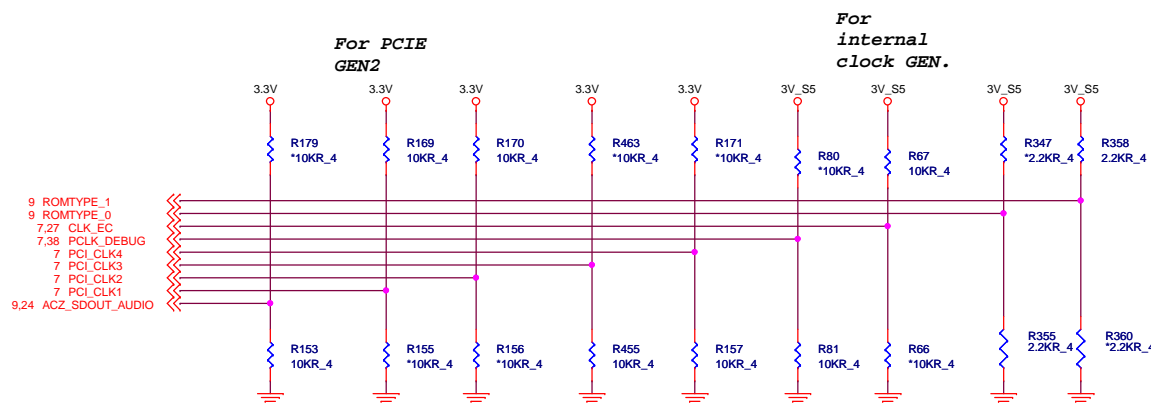




REQUIRED STRAPS



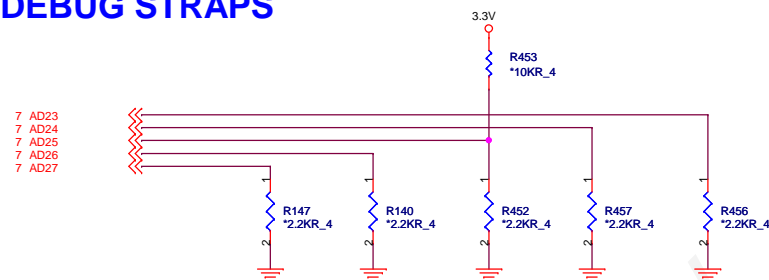
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



	ACZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	INT_EC_EN	INT_CLK_EN	ROMTYPE_1/0
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enable DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK MODE	INTERNAL EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disable	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE DEFAULT	INTERNAL EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM L, L=FWH ROM

internal have pull Hi 10K

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT



Quanta Computer Inc.

PROJECT : QUD(C225)

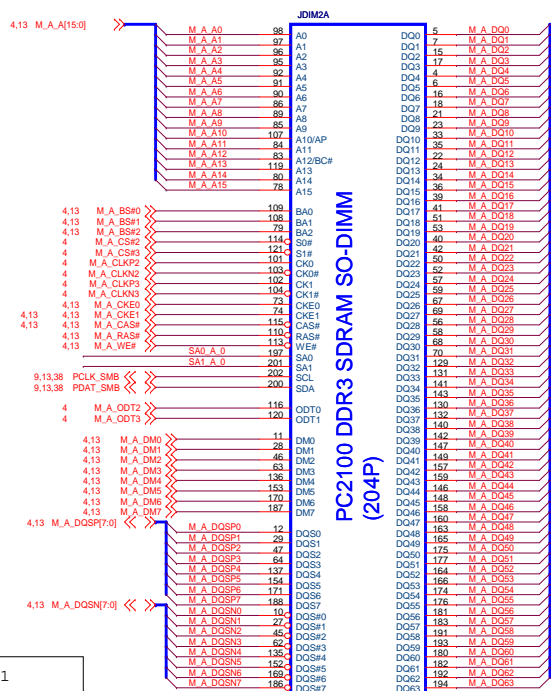
Size Document Number

STRAPS/PWRGD

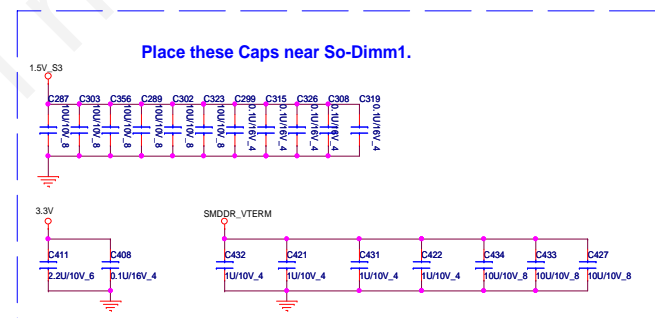
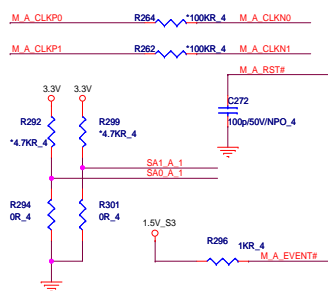
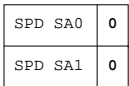
Date: Wednesday, May 18, 2011 Sheet 11 of 37

Rev A

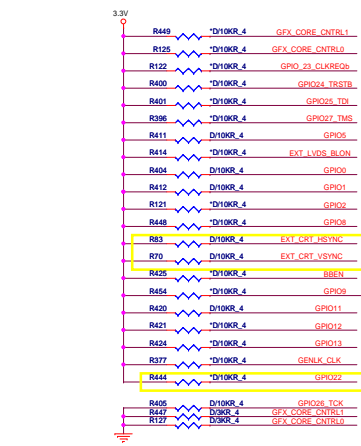
CHANNEL A DIMM 1 H5.2

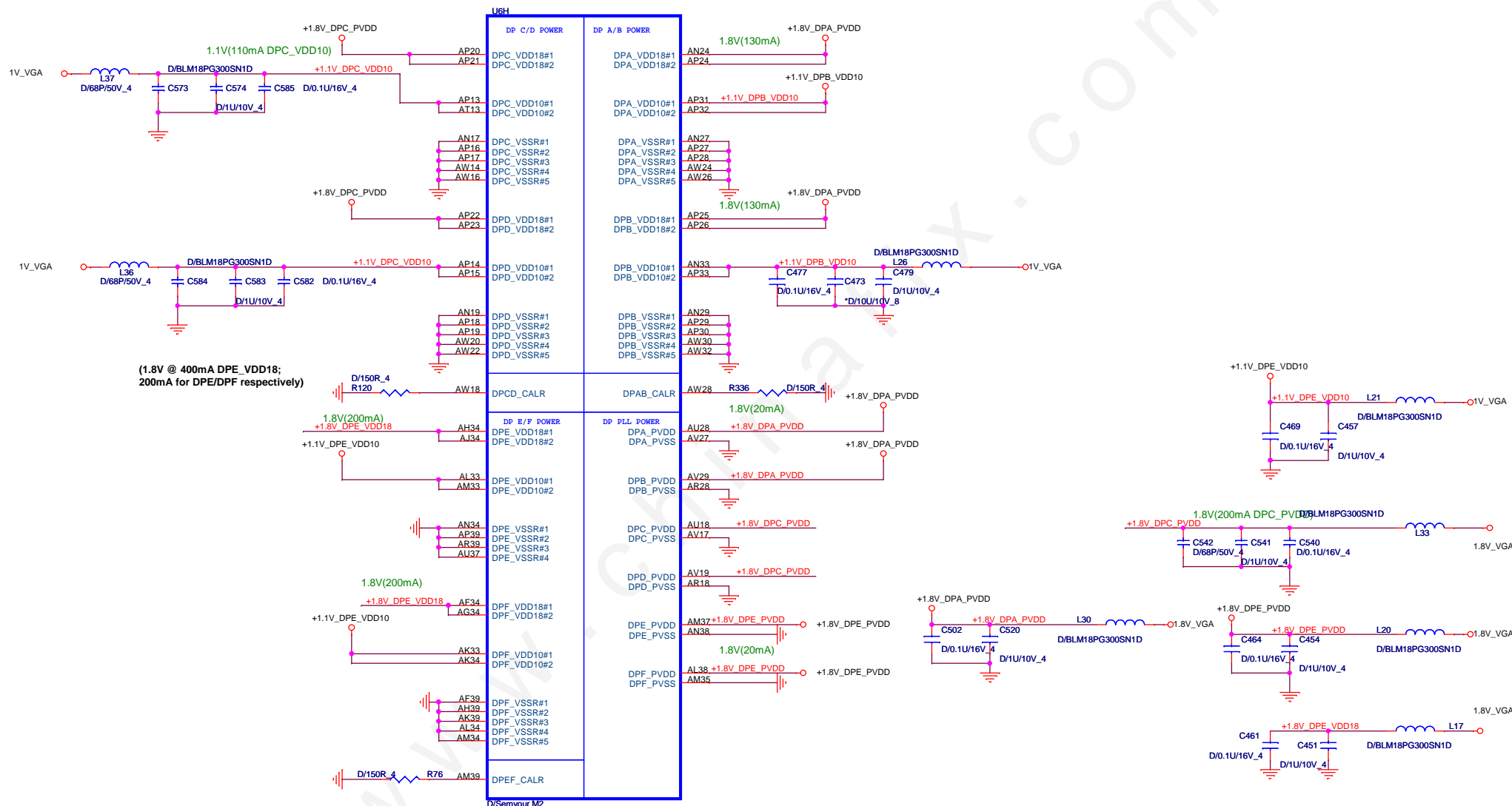


4,12 M_A_A[15:0] >> M_A_A0

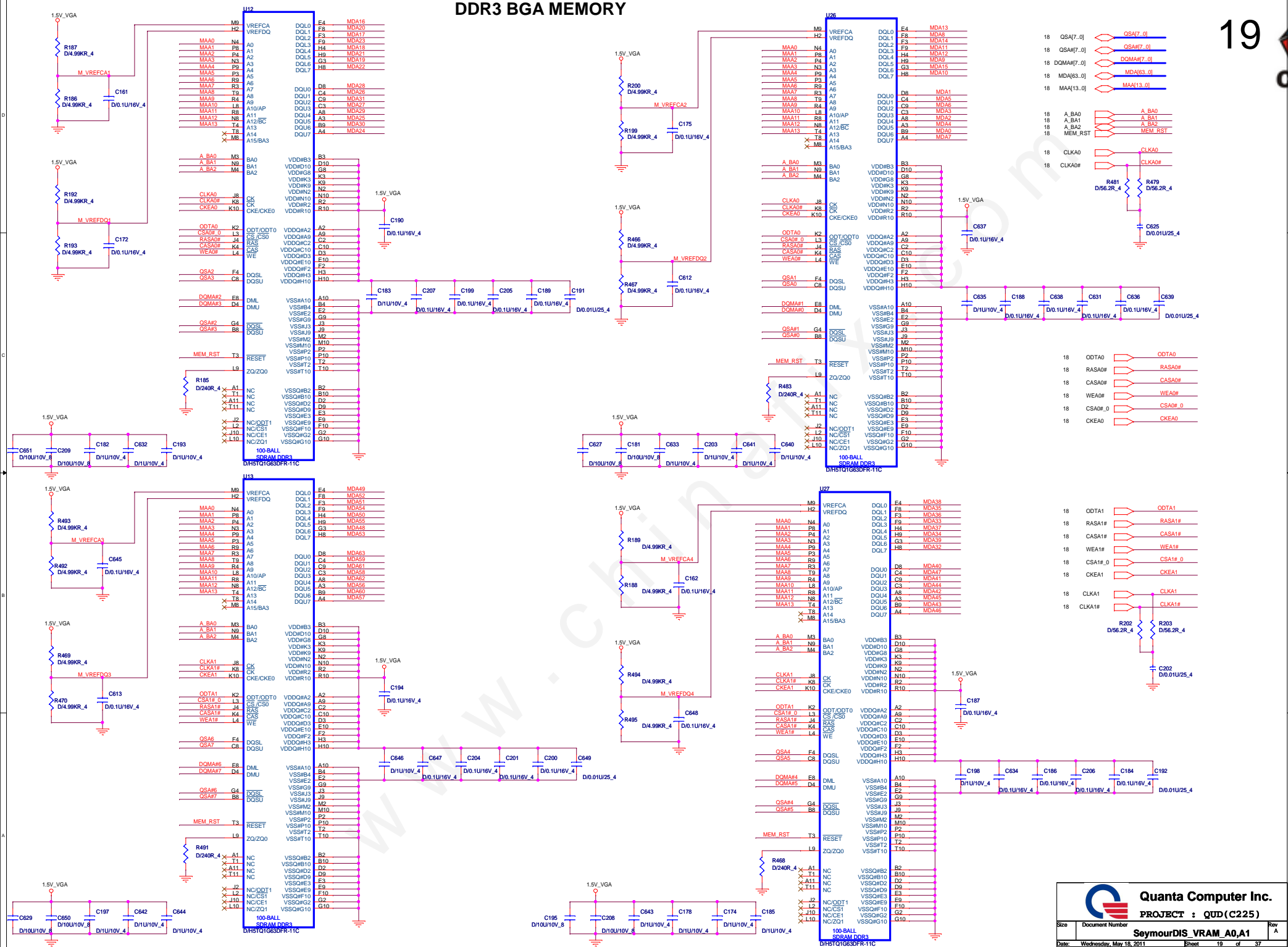


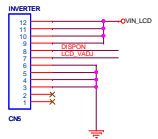
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
STRAPS	Name	DESCRIPTION OF DEFAULT SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 2.5 V output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 Gb/s capable at power-on. 1 = Advertises the PCIe device as 5.0 Gb/s capable at power-on. Note: 5.0 Gb/s capability will be controlled by software.
BIF_VGA_DIS	GPIO9	VGA Disable determines whether or not the card will be recognized as the system's VGA controller. 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller
BIOS_ROM_EN	GPIO22	ENABLE EXTERNAL BIOS ROM 1:enable 0:disable
ROMCFG2(2:0)	GPIO[13:11]	Primary Memory Aperture size requested Size of the primary memory apertures CONFIG2(2:0) 128 MB 000 256 MB 001 512 MB 010 1 GB 011 Note: For frame buffers larger than 256 MB (e.g. 512 MB, 1 GB) the aperture size should be 256 MB.
VIP_DEVICE_STRAP_ENA	DAC2_VSY	IGNORE VIP DEVICE STRAPS 1:enable 0:disable
AUD[1] AUD[0]	EXT_CRT_HS_VSYNC EXT_CRT_VSYNC	AUD[1] AUD[0] 0: 0 No audio function 1: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 1 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI
RSVD RSVD RSVD	GPIO8 GPIO_21_BB_EN GENCLK_CLK	Internal use only. Internal use only. Internal use only.



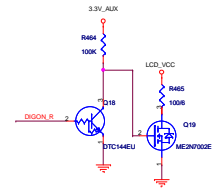


19

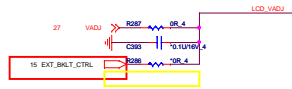
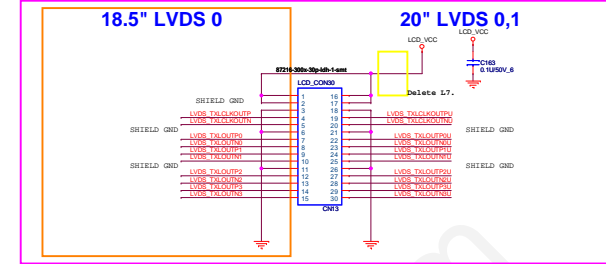




PN:DPWF40MS017

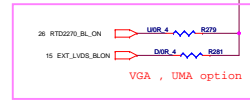
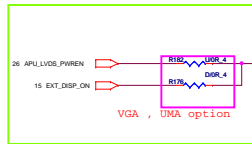


LCDVCC Discharge Circuit

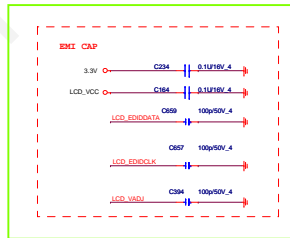
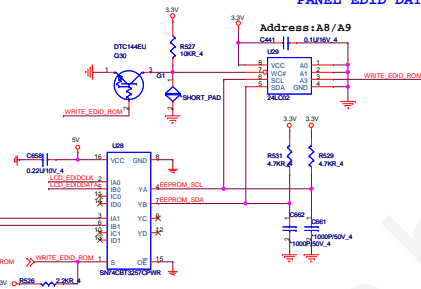
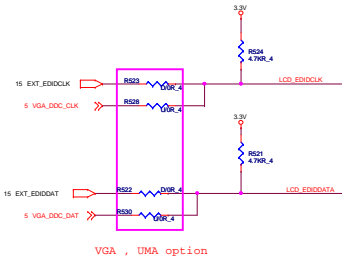


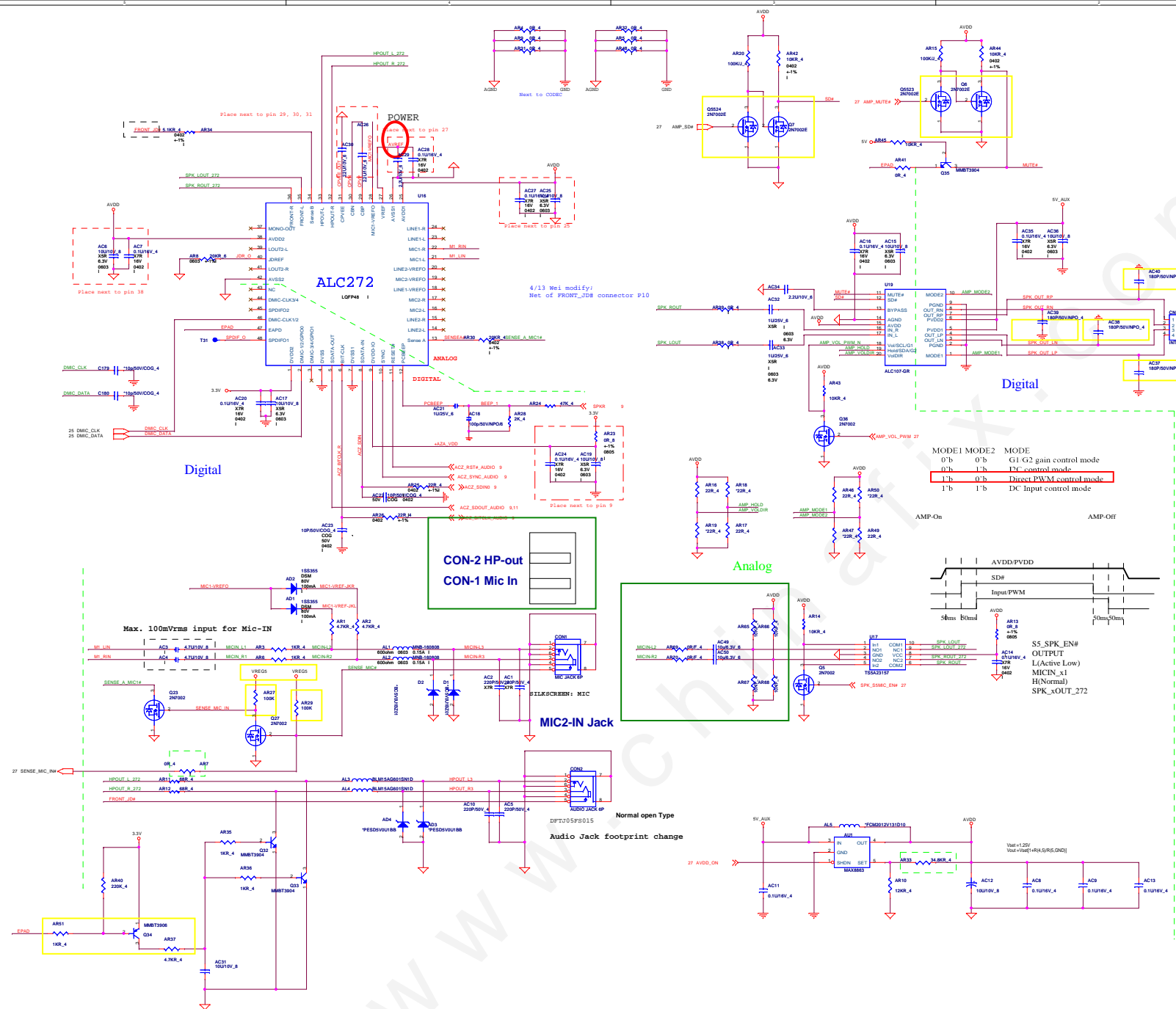
PANEL VCC CONTROL

PANEL BACKLIGHT CONTROL

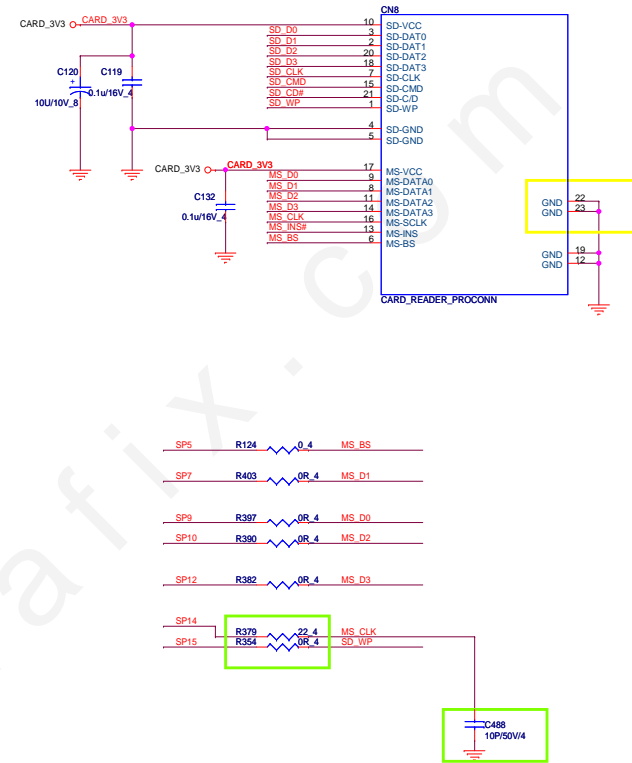
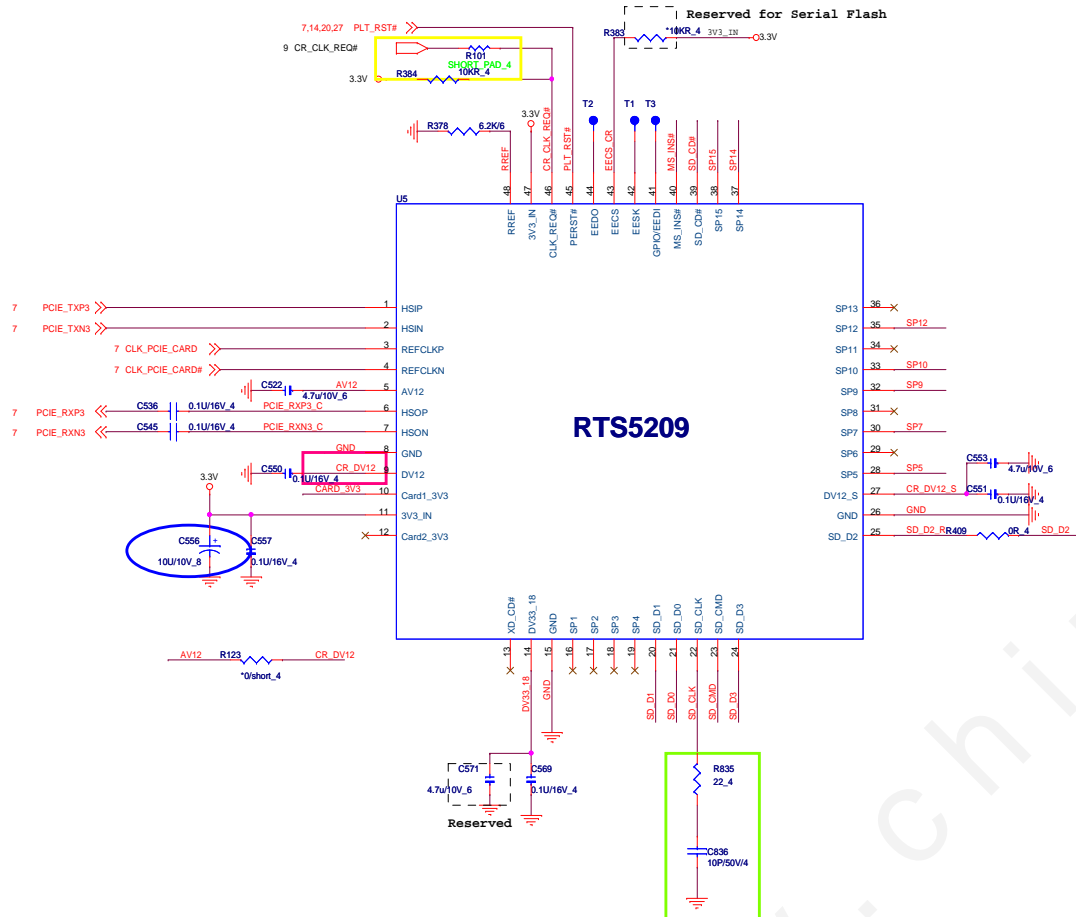


EEPROM IIC Selection
PANEL EDID DATA



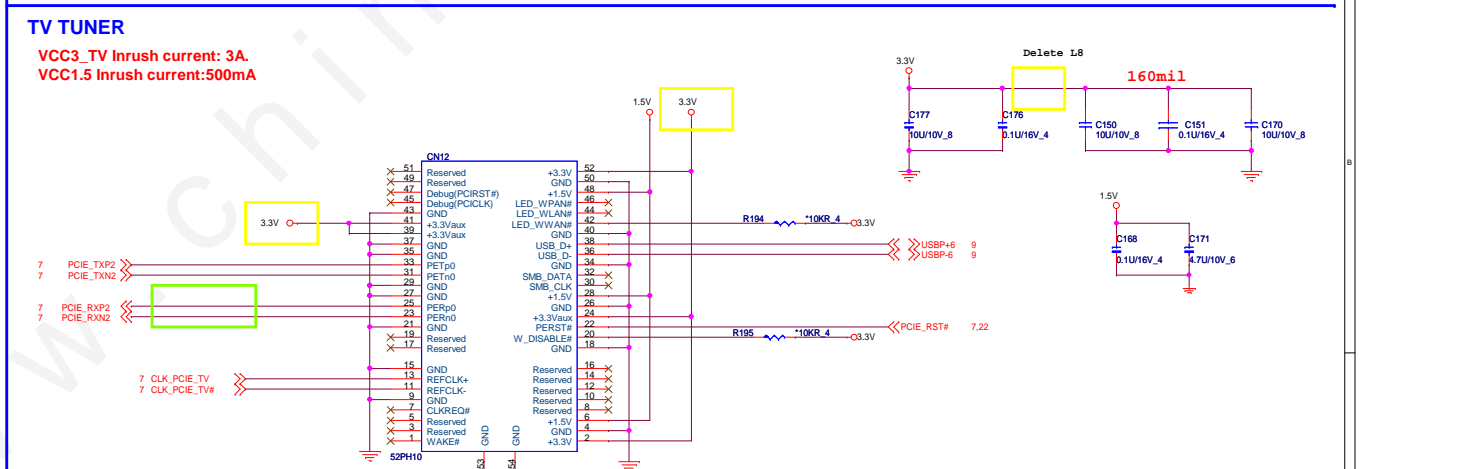
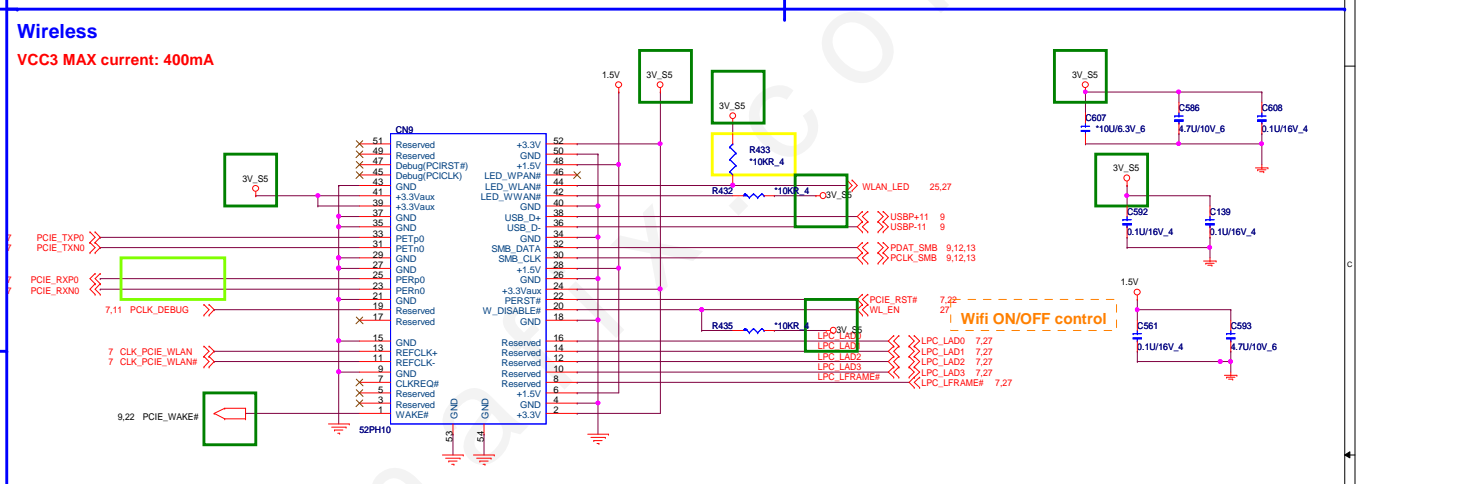
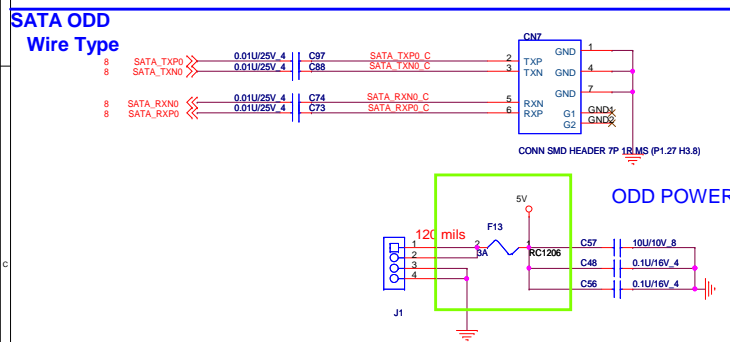
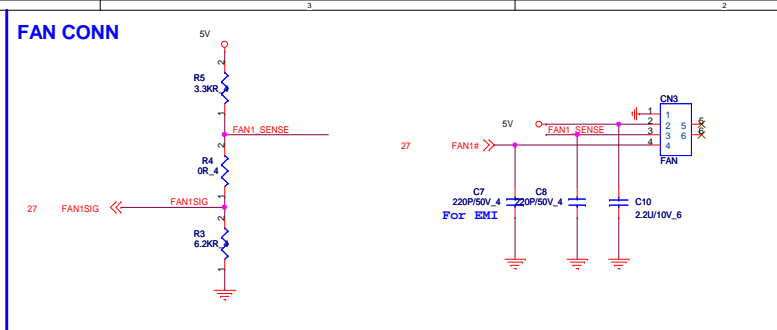
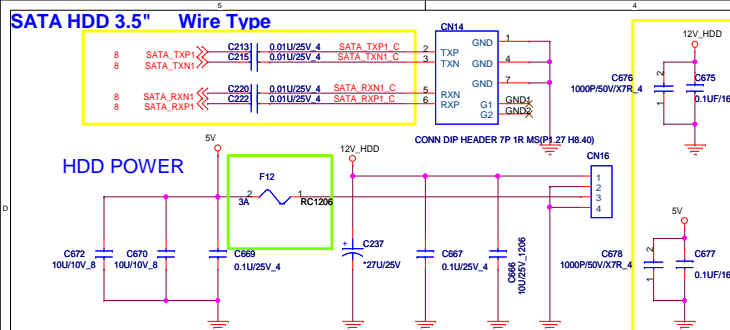


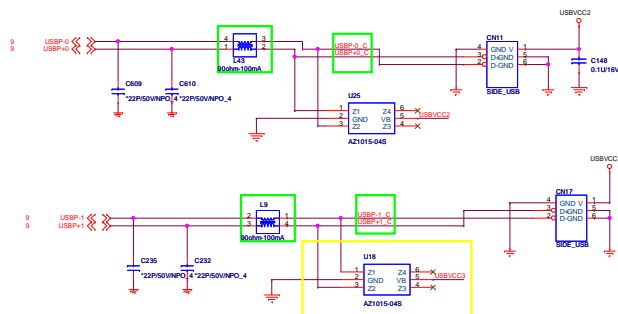
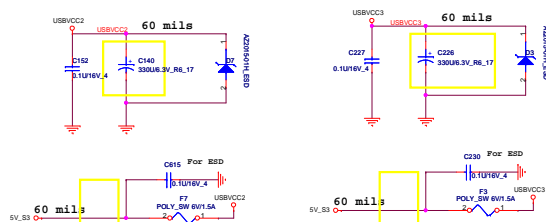
4 IN 1 CARD READER



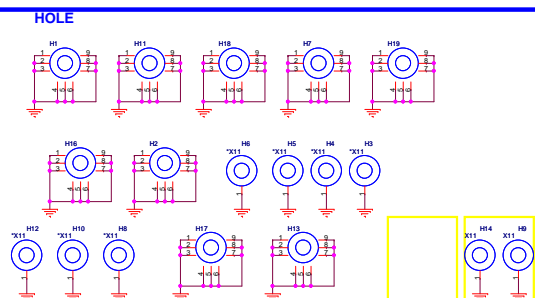
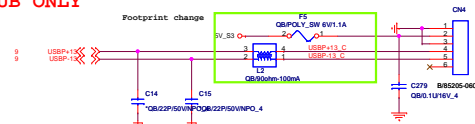
Share Pin

Share Pin	XD	MS	SD
SP1	XD_R/#		SD_D7
SP2	XD_RE#		SD_D6
SP3	XD_CE#		SD_D5
SP4	XD_WE#		SD_D4
SP5	XD_CLE	MS_BS	
SP6	XD_ALE	MS_D5	
SP7	XD_WP	MS_D1	
SP8	XD_D0	MS_D4	
SP9	XD_D1	MS_D0	
SP10	XD_D2	MS_D2	
SP11	XD_D3	MS_D6	
SP12	XD_D4	MS_D3	
SP13	XD_D5	MS_D7	
SP14	XD_D6	MS_CLK	
SP15	XD_D7		SD_WP

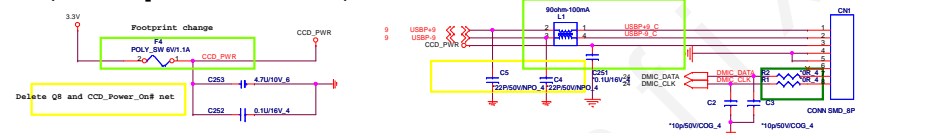




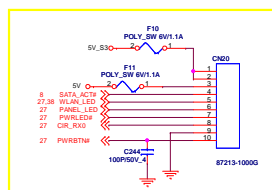
Touch Panel (Define by EETI module)
QUB ONLY



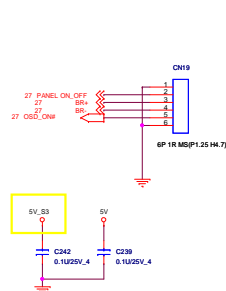
WEB CAM MODULE 113mA
(Define by Bison CCD module)



POWER SWITCH/LED

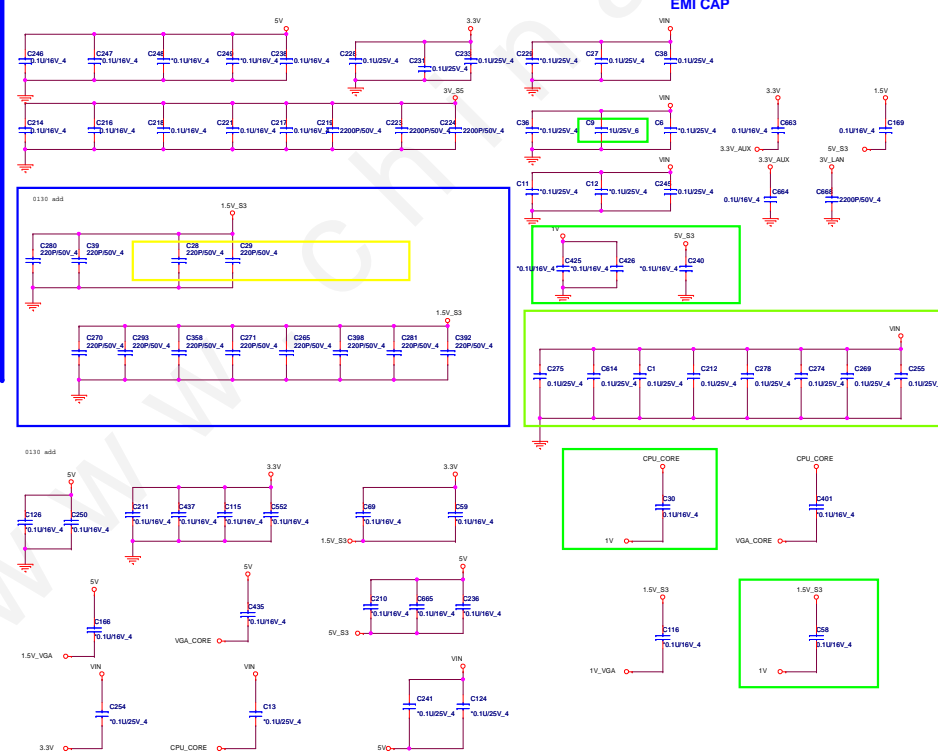
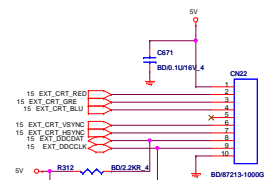


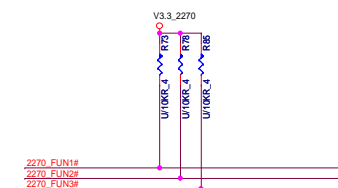
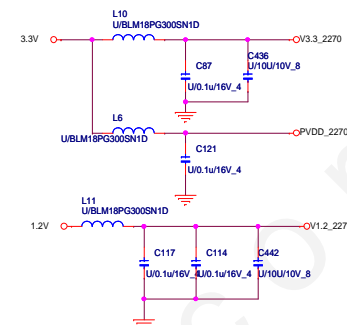
FUNCTION BUTTON BOARD

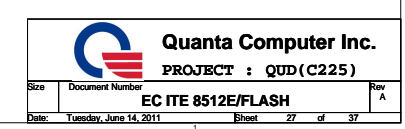


UMA CRT FOR DEBUG

Discrete CRT for Debug





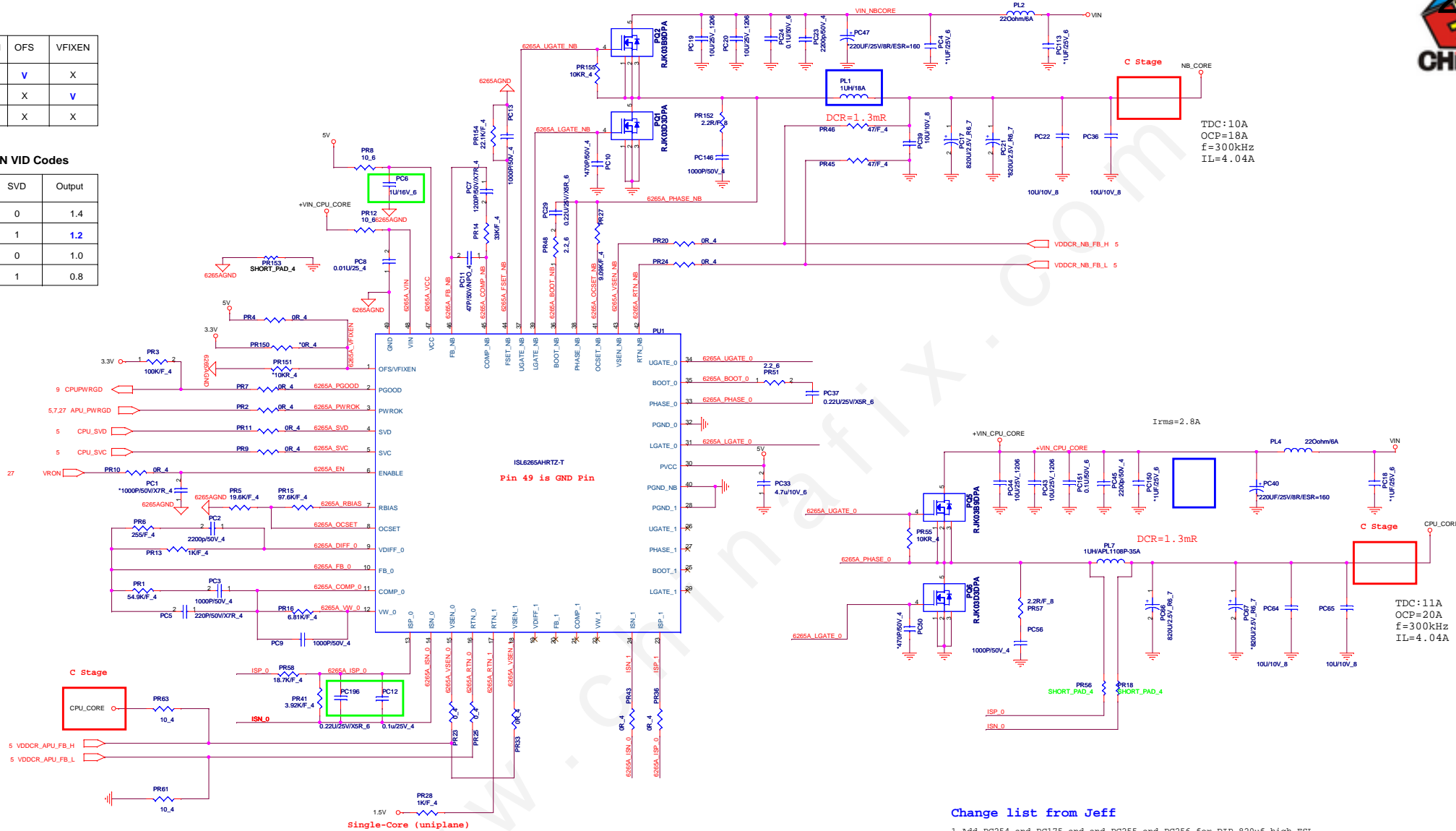




ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

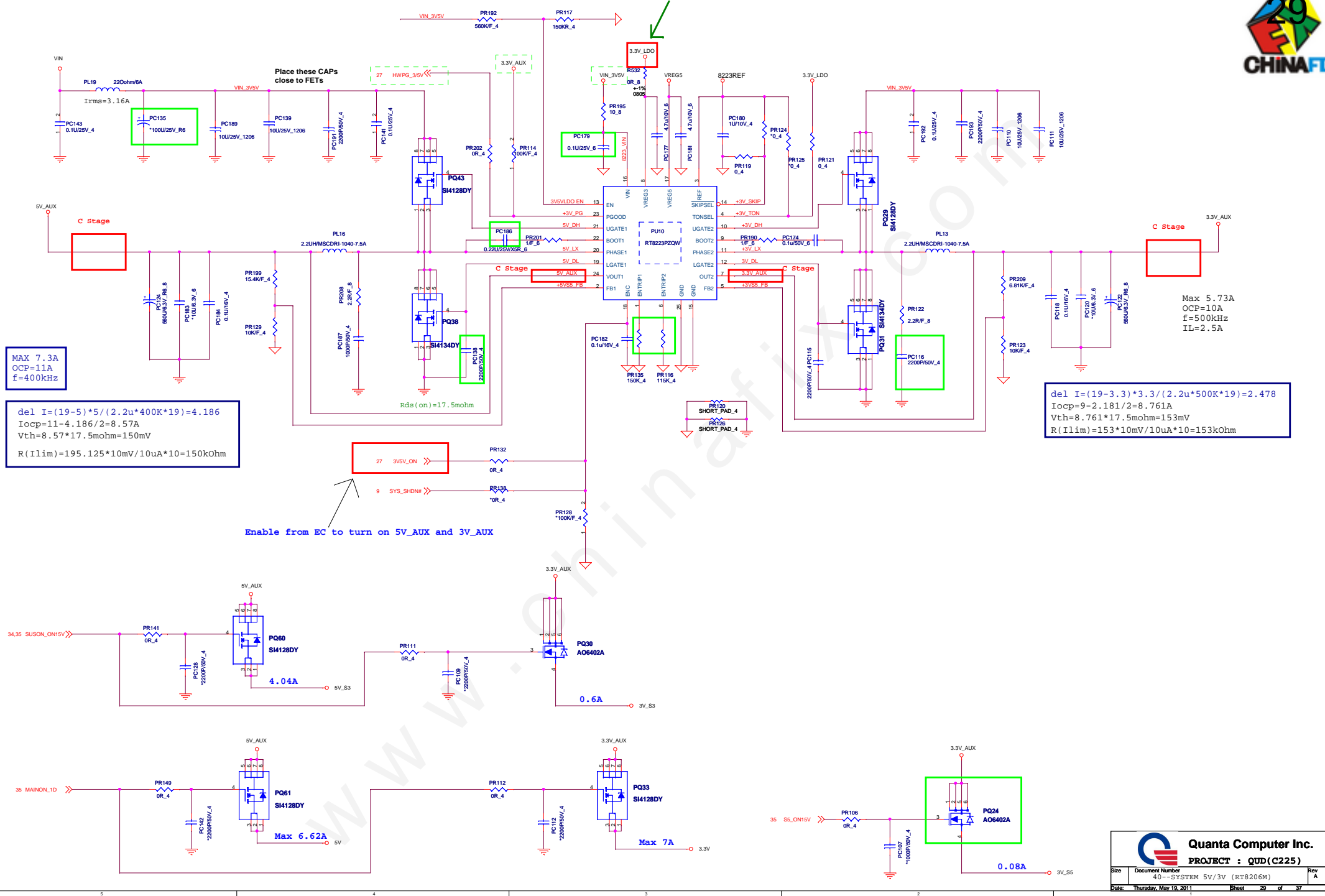
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



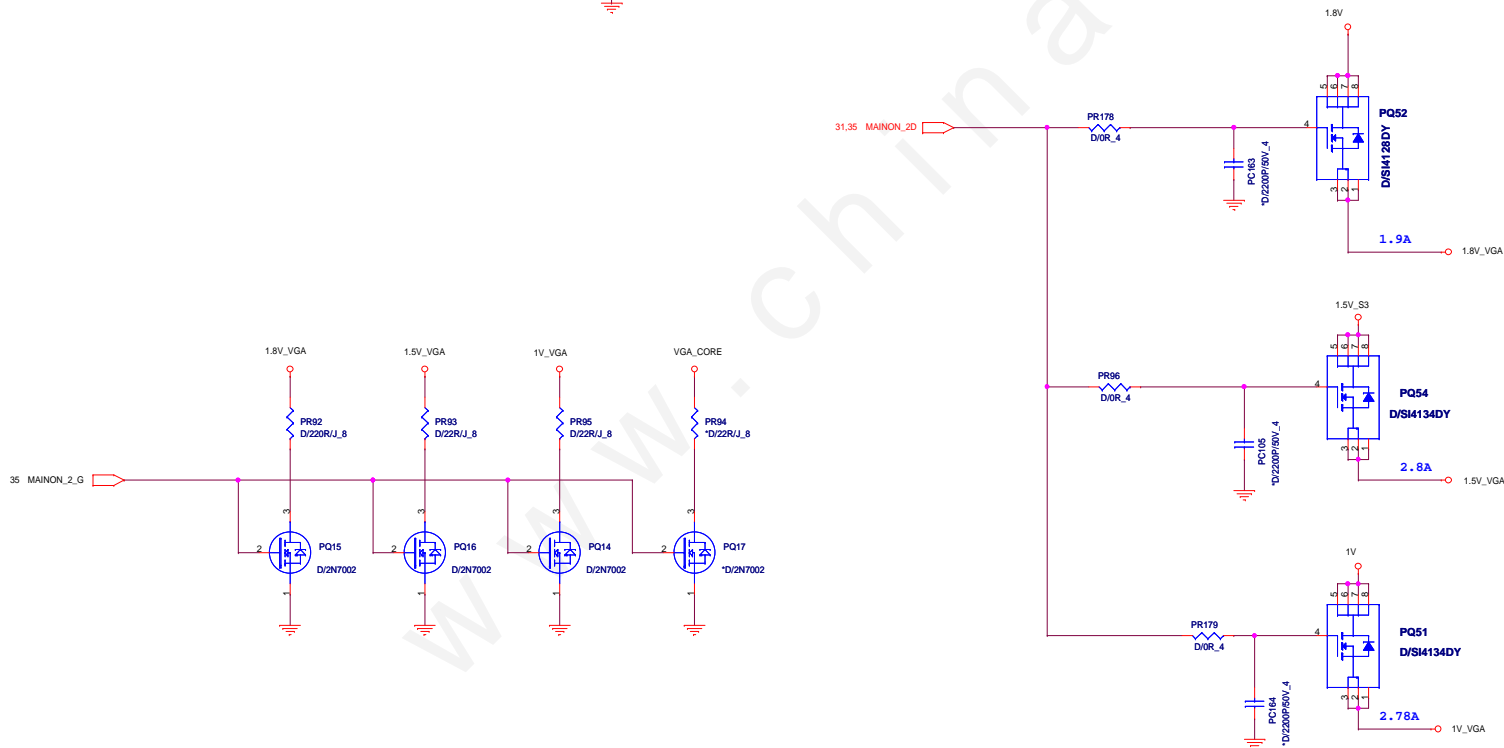
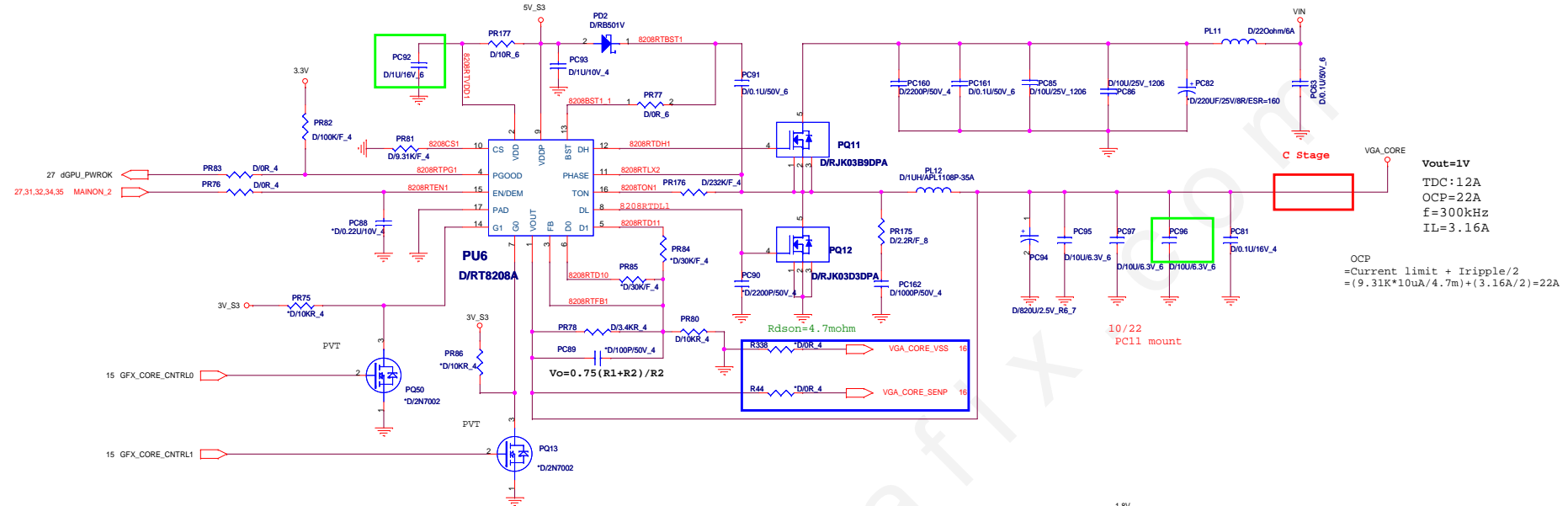
Change list from Jeff

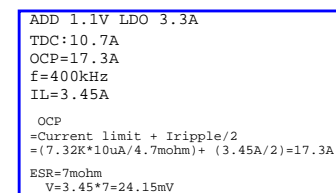
- 1.Add PC254 and PC175 and and PC255 and PC256 for DIP 820uf high ESL
- 2.Add PC254 and PC175 for DIP 820uf high ESL
- 3.Delete PC234 at output CPU_CORE
- 4.Delete PR160,PR161,PR162,PR163 at High Side gate resistor 0 ohm.
- 5.PC229 move to PL13 "net +VIN_CPU_CORE"
- 6.ADD PC257 for capacity

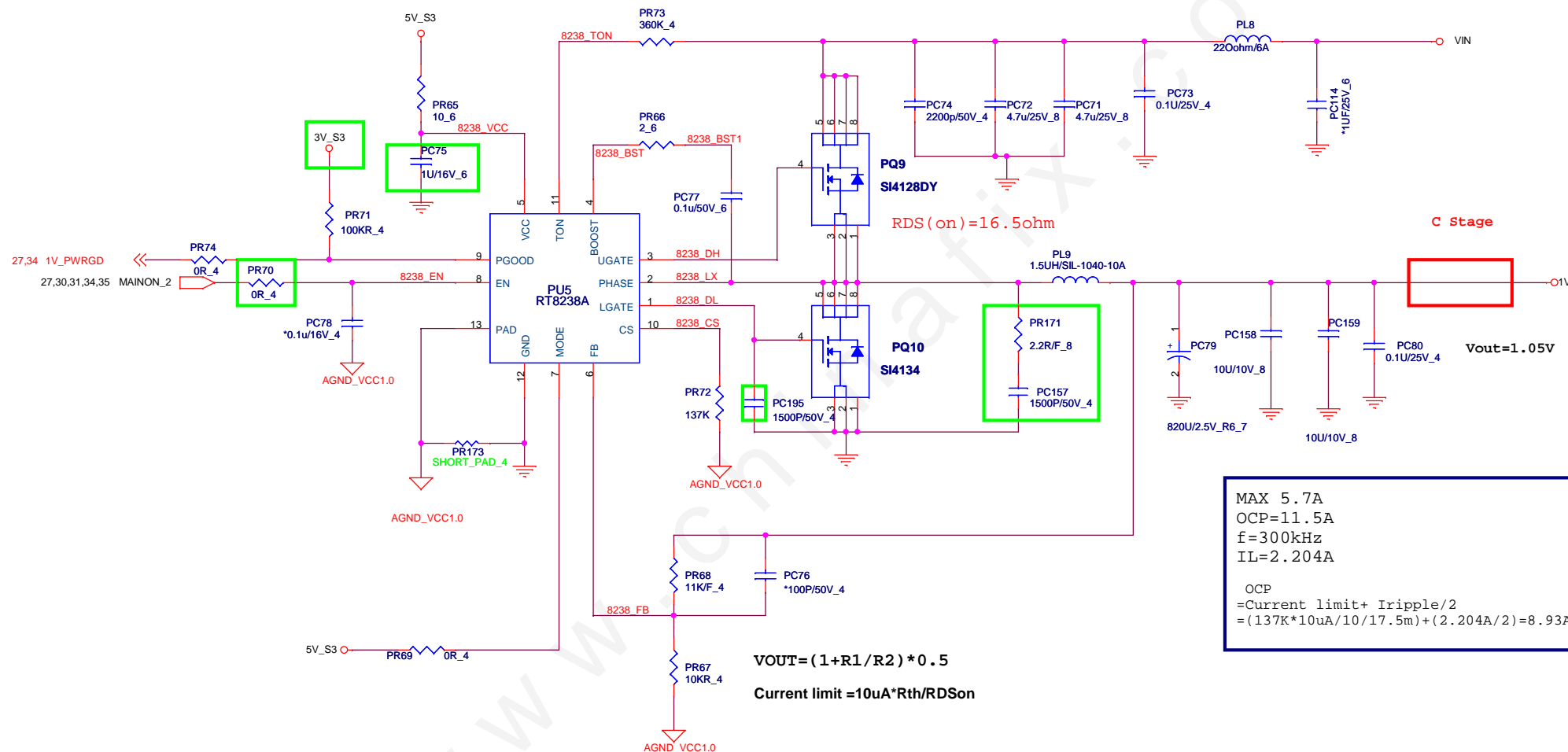
VREG3 only for EC power which max current under 50mA



VGA Core

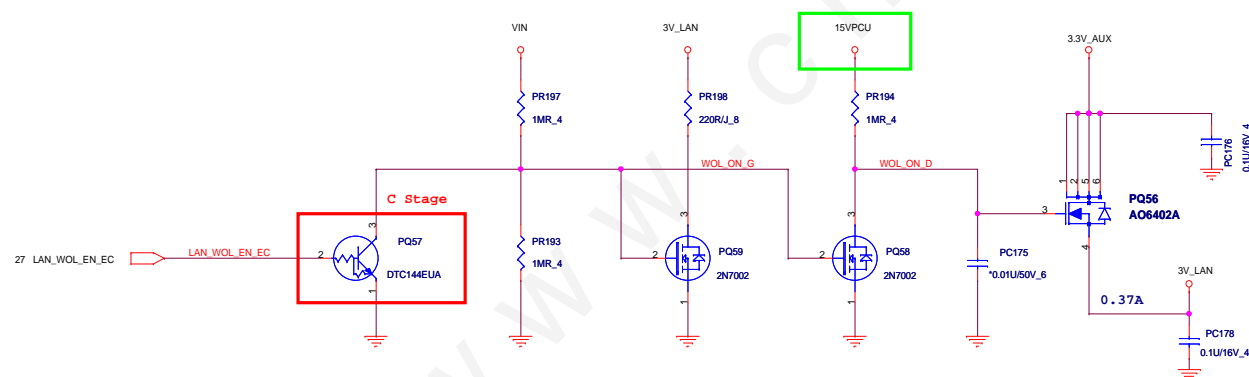
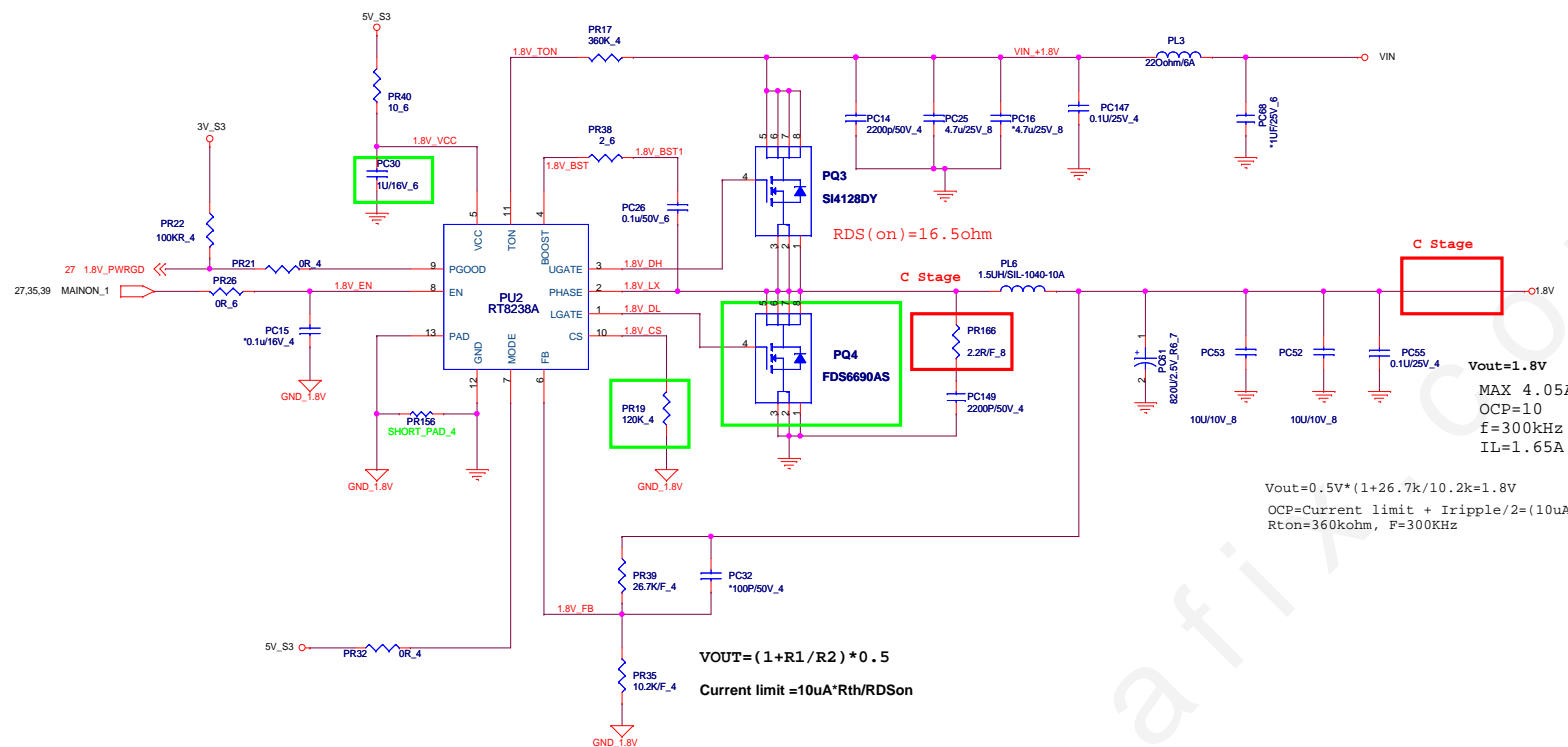


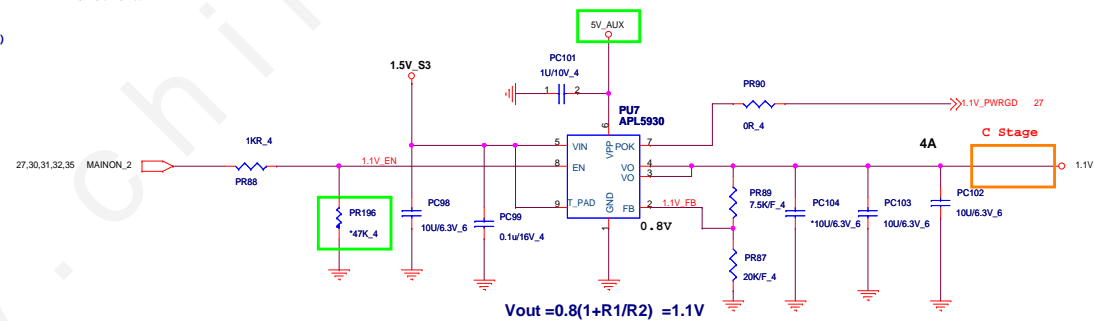
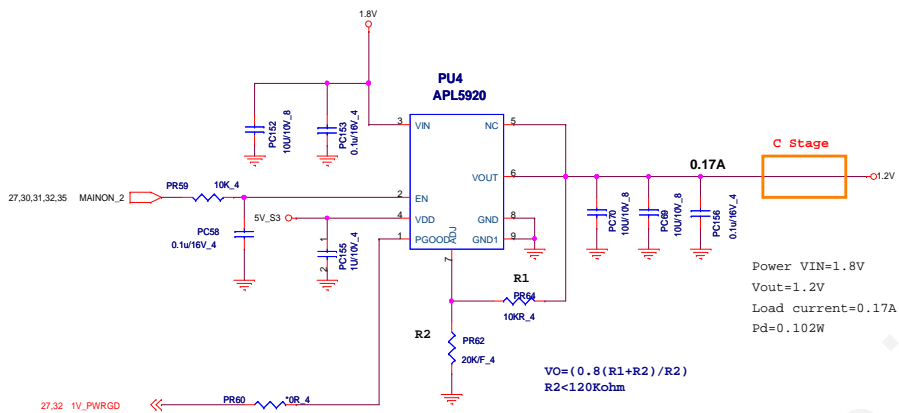
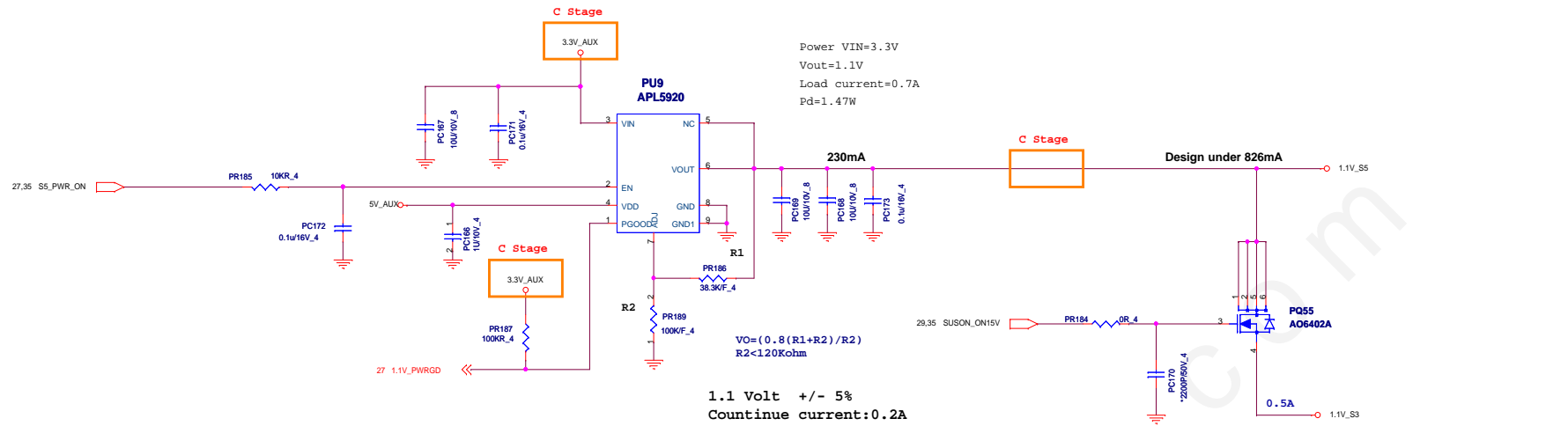

$$\begin{aligned} \text{OCP} &= \text{Current limit} + I_{\text{ripple}}/2 \\ &= (5.1\text{K} \cdot 10\mu\text{A} / 4.7\text{mohm}) + (2.3\text{A} / 2) = 12\text{A} \end{aligned}$$



Quanta Computer Inc.
PROJECT : QCU (C205)

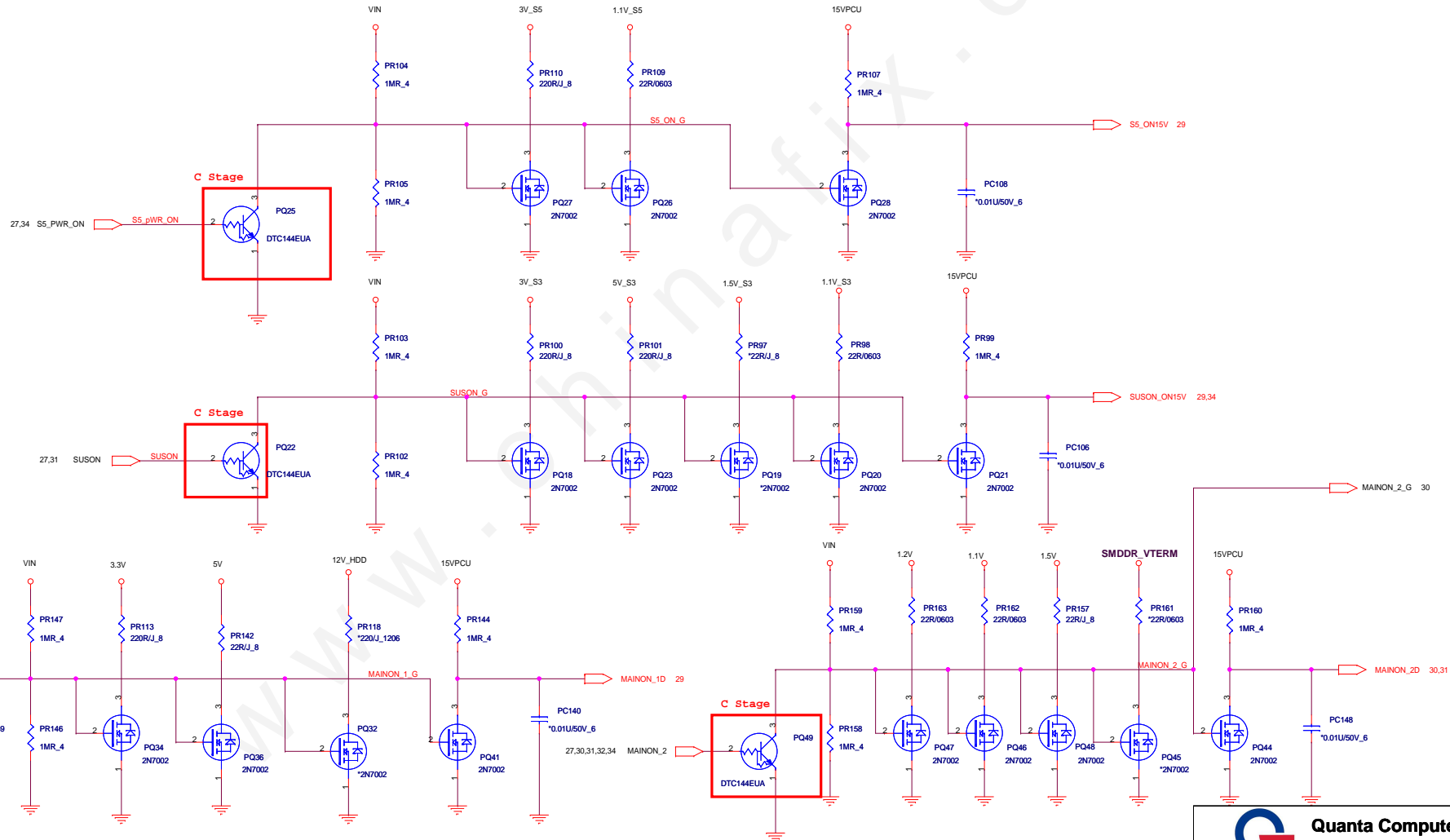
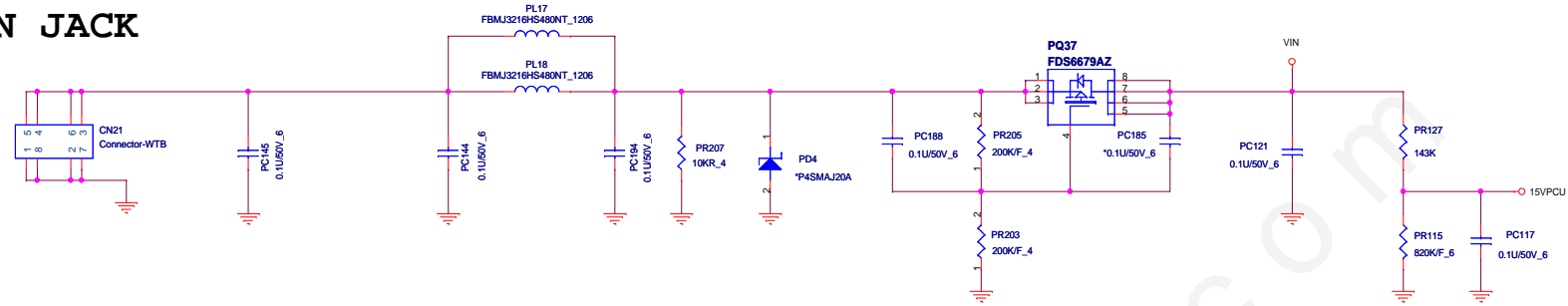
Size	Document Number	Rev
	VCC1.0(RT8202A)	4D
Date:	Wednesday, May 18, 2011	Sheet 32 of 37





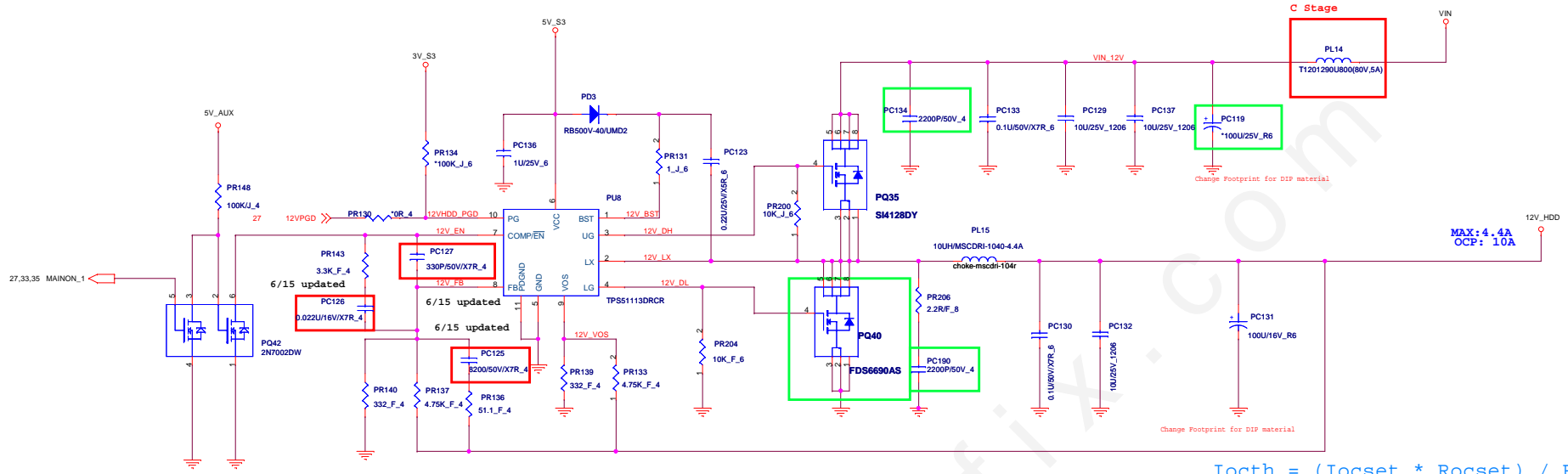
ramp-up time for all power rails
50 us <All power rails except 5V_S5 <40 ms
100 us <5V_S5<40 ms

DC IN JACK



Quanta Computer Inc.
PROJECT : QCU(C205)

HDD_12V



$$I_{octh} = (I_{ocset} * R_{ocset}) / R_{ds(on)}$$

$FDS6690 R_{ds(on)} = 15 \text{ m ohm}$
 $I_{ocset} = 10 \text{ uA}$
 $R_{ocset} = 15 \text{ k ohm}$
 $I_{octh} = (10 \text{ uA} * 15 \text{ k}) / 15 \text{ m ohm} = 6.667 \text{ A}$

1.Reserve U22,U23,C400,C365-For debug use.
2.Reserve R19 and Mount R18-Enable HDMI function.
3.Reserve/short R289,R290,R297,R302,R6.
4.D5 power source change to 3.3V LDO
5.Reserve/Short R184,R160,R337,R398,R321,R117,R389.
6.Delete L8 and Change 3.3V_TV power source to 3.3V
7.Add C3170,C3171,Y5,R808,R809,R8011,R8012,R8013.
8.Delete Q8 and CCD_Power_on# net
9.Reserve C5,C4.
10.Delete R434,R426,R423,R422,R415.
11.Delete LED1-LED6, Q9-Q13, R304-R309 for debug use.
12. Change C242 power source to 5V_S3.
13.Delete L7,C243,C225.
14. Change CN20 pin1 power to 5V_S3, pin 2 to VCC5 and delete pin8 CIR_RX0 net.
15.Add F10,F11 for safety concern.
16.Change C140,C226 footprint.
17. Del R172 not mount
18. Del R275 not mount
19. R7 from 150 ohm change to 499 ohm
20. MB_HDMI_DDCCLK change link to CN15[B18]
21. MB_HDMI_DDCDATA change link to CN15[B19]
22. Change CN7 footprint
23. Change J1 footprint
24. Change CN14 footprint
25. Change CN16 footprint
26. Change CN11,CN17 footprint
27. Change CON1, CON2 footprint

power 3/22

28.change PC87 to SMT type
29.PC138,PC184,PC116,PC149,PC134,PC190change to 2200PF
30.PK70 change to 0402 type
31.PR171,PR166 mount 2.2 ohm,PC151 1500PF
32.add PC19(1500pf)
33.add PC163(0.22uf)
33.PR135 change to 150K
34.PR116 change to 115K
35.FU7 pull low 47K.
36.delete PC100
37.PQ4,PQ40 change to FDS6690AS
38. PR19 change to 120K
39.PC96 change to 0603 type
40.FU7 pin6 change net to 3V_AUX
41.PR71 pull high change to 3V_S3
42.PC179 change to 0603 type
43.PC6,PC92,PC38,PC35,PC75,PC30 change to 0603 type

3/25 update

44. Add D26,D27,D28,D29 diodes
45. Change U18 AZ1015-048
46. CN18 add Pin 22, 23 link to GND
47. Change AR29 to 100K ohm
48. Change power net from AVDD to VREG5
49. Change Q6,Q7 add Q5523, Q5524 2N7002
50. 12V_HDD add C675,C676 for EMI
51. 5V add C677,C678 for EMI
52. CN14 change link [2]SATA_RXP1_C
53. CN14 change link [3]SATA_RXN1_C
54. CN14 change link [5]SATA_TXN1_C
55. CN14 change link [6]SATA_TXP1_C
3/28 update
56. Del APU_VADJ_2130S net, R288, R64,SW1, R69, R91 for Adj/WB
57. Del R8218, R79, FCH_14318M_CR net use external crystal for Scalar
58. Short pad R101
59. Reserve R433,
60. Change C226,C140 to 330U/6.3V_R6_17 SMD type
61. Change H1 footprint to hg-c276d138p2
62. Change R462 footprint to short0603.
63. Add R536, R537, R538, R539 reserved resister for EMI
64. Remove DDR window component. (C25, C26, C55, C33, C34)
65. Del H15 for DXF
3/29 update
66. D26,D27,D28,D29 change to 1S8355
67. Change R8011,R8012,R8013 to 75ohm
68. AR27 change to 100k ohm
69. Add CIR_RX0 net
70. CN21 change footprint for layout vicky
71.Add AR51 1K ohm for decrease current when power on.
72.Add R8014,R8015 and Q5525 for HDMI hot plug detect for Discrete SKU.
3/30 update
73. H13 change footprint
4/1
74. CN14 change link [2]SATA_TXP1_C
75. CN14 change link [3]SATA_TXN1_C
76. CN14 change link [5]SATA_RXN1_C
77. CN14 change link [6]SATA_RXP1_C
4/17
78. Change power net name FU9[3], PR187[1]from 3V_AUX to 3.3V_AUX
79. Modify DDR page need to mount the parts
4/27
80. Del USB_OC function, D28,R235,R236,PR108, USB_OC7#_R
81. Del USB_OC function, D29,R131,R132,PR182, USB_OC4#_R
82. Del USB_OC function, C673,F2,D26, R225,R220, PR181 USB_OC5#_R
83. Del USB_OC function, C674,F1,D27, R224,R219, PR183 USB_OC6#_R

5/08 update
84. Reserve DMICInterface R1,R2,C2,C3
85. R184 footprint change to Short0402
86. OSD_ON# add 4.7K ohm R810 pull up to 3.3V
87. EC Pin 69 2270_FUN1# move to EC pin 16
88. EC Pin 70 2270_FUN2# move to EC pin 120
89. EC Pin 71 2270_FUN3# move to EC pin 115
90. EC_PHYSICS (R490)and EC_WHITE(R487)3.3V_LDO power change to 3.3V
91. Reserve CON3
92. Reserve R480 WL_EN Pull up resister
93. WLAN change power from 3.3V change to 3V_S5
94. Add audio bias voltage AR65.AR66,AR67,AR68,AR69, AR70,AC49,AC50

5/11 update Jeff

84. PR166 chang to 0805 type
85. PLL14 change PN which vendor TTY
86. PC87 change to 330uF and add PC197
87. PQ22,PQ25,PQ39,PQ49, PQ57 change PW
88. Delete PR164,PR167,PR174,PR145,PR168,PR169,PR172,PR198,PR191,PR79,PR91
5/11 Anson
89. CN9 Pin1 lin to PCIE_WAKE#
90. R435 change to 3V_S5
91. R432 change to 3V_S5
92. R536,R537,R538,R539 change to 150 ohm
93. R6 remove to BOM(short pad)
94. EC pin 73 link to R811,R812

R0C-->R0D

6/09
95. Del U8 TC7SH08FU
96. Add fuse at HDD/ODD 5V power for 3C test
97. Modify NUT P/N to MBQU1002010 for H9, H14 location
98. Add U34,U35 EEPROM Co-lay

power 6/15

99. PC127 change to 330p
100. PC126 change to 0.022uf
101. PC125 change to 8200pf
6/17
102. CN7 change footprint to sata-ld1107f-s33t5-7p-r